

RELIABILITY TEST RESULTS

High Temperature Storage (125°C)

The High Temperature Storage test was performed to accelerate failure mechanisms that are primarily thermally activated (such as ionic diffusion through the passivation) and to age the polyimide coating. The devices under test (DUTs) were stressed in accordance with JESD22-A103 at 125°C for a duration of 1000 hours. The samples were periodically removed from stress at the indicated readpoints and retested to the Final Test as well as with PC test to check for degradation. No device degradation or failures were detected by this testing.

Table 1. High Temperature Storage Test Results

Lot	168 Hrs	500 Hrs	1000 Hrs
1	0/45	0/45	0/45
2	0/45	0/45	0/45
3	0/45	0/45	0/45
TOTAL	0/135	0/135	0/135

High Temperature Operating Life (100°C, 6.0V)

The High Temperature Operating Life test was performed to accelerate a wide range of semiconductor failure mechanisms that are activated by increasing temperature and bias voltage. The DUTs were exercised during this stress by a stimulus test pattern that repeatedly writes the digital registers and scans the pixel array to simulate operation. The devices were stressed in accordance with JESD22-A47, operating in a 100°C ambient at 6.0 volts, for 1000 hours. The samples were periodically removed from stress and retested to check for degradation as described above.

Table 2. High Temperature Operating Life Test Results

Lot	168 Hrs	500 Hrs	1000 Hrs
1	0/45	0/45	0/45
2	0/45	0/45	0/45
3	0 / 44 ⁽¹⁾	0/44	0/44
TOTAL	0/134	0/134	0/134

Note 1: One device was damaged by handling, however, no chargeable failures or device degradation was observed during this testing.

Temperature Humidity Bias (85°C, 85% RH, 5.5V)

The 85/85 Temperature Humidity Bias test was performed to accelerate the galvanic corrosion and leakage effects from moisture and electrical bias. The test samples were stressed per JESD22-A101-B at 85°C and 85% Relative Humidity, with 5.5 volt static bias applied. The samples were periodically removed from stress and retested to check for degradation as previously described. This test produced no failures, evidence of corrosion, or other degradation of the devices.

Table 3. T.H.B. Test Results

Lot	137 Hrs	548 Hrs
1	0/35	0/35
2	0/29	0/29
3	0/36	0/36
TOTAL	0/100	0/100

Temperature Humidity Storage (130°C, 85% RH)

HAST is a widely used stress for assessing the moisture resistance of plastic encapsulated devices and is particularly important to the BioSlimDisk iCool products since the silicon chip is exposed to the environment. This stress is performed at an unsaturated condition of 130°C and 85% RH, and 33 PSIA (without electrical bias). This stress is very effective for accelerating moisture-induced failures arising from defects in the passivation films or delamination between films. This stress was performed for 192 hours. No changes to the image or other device degradation was detected in this test.

Table 4. H.A.S.T. Test Results

Lot	96 Hrs	192 Hrs
1	0/45	0/45
2	0/45	0/45
3	0/45	0/45
TOTAL	0/135	0/135

Temperature Cycling Test

Temperature cycling was performed to accelerate the effects of the thermal expansion mismatch between the different materials within the module and to check the integrity of the wire bonds, component attach, and solder joints. This testing was performed in accordance with JESD22-A104B, at a rate of two cycles per hour. Two different test conditions were used including -20°C to $+85^{\circ}\text{C}$ (105°C Δ) and -40°C to $+125^{\circ}\text{C}$ (165°C Δ).

Table 5. -20°C to $+85^{\circ}\text{C}$ Temperature Cycling Test

Lot	100 Cys	500 Cys	1000 Cys	1500 Cys
1	0/32	0/32	0/32	0/32
2	0/19	0/19	0/19	0/19
3	0/36	0/36	0/36	0/36
4	0/16	0/16	0/16	0/16
5	0/24	0/24	0/24	0/24
6	0/8	0/8	0/8	0/8
TOTAL	0/135	0/135	0/135	0/135

Table 6. -40°C to $+125^{\circ}\text{C}$ Temperature Cycling Test

Lot	100 Cys	500 Cys
1	0/32	0/32
2	0/19	0/19
3	0/36	0/36
4	0/16	0/16
5	0/24	0/24
6	0/8	0/7 (Note 1)
TOTAL	0/135	0/134

Note 1: One device failed continuity on NRST pin. Physical analysis determined that the substrate trace connecting the external test point was cracked as it passed under the edge of the die. The device was verified to pass all tests through the connector, and is not considered to be a chargeable failure.

Sensor Electrostatic Discharge (1500Ω, 100 PF RC NETWORK) (ESD)

The Sensor surface ESD sensitivity testing was performed in accordance with IEC 61000-4-2 using a Schaffner NSG 435 ESD Simulator equipped with the INA 425 RC Discharge network (100pF, 1500 ohm) and test finger. This RC network best represents the pulse that can be expected for a person touching the sensor array. Air discharge test were conducted with discharges at +/- 15,000 volts. Each device was subjected to 10 ESD discharge pulses at the specified stress voltage, and was tested after each zap using the PC test program for factory level and current Gateway Suite program for application level.

Table 7. Sensor Electrostatic Discharge (ESD) Test Results

# of Sample Devices	Stress	Grade A Factory Level	Grade B Application Level
11	- 15KV, 10 Zaps	8/11	0/11
2	+ 15KV, 10 Zaps	2/10	0/10

Pins Electrostatic Discharge (1500Ω, 100 PF RC NETWORK) (ESD)

The pins of the BioSlimDisk iCool module were subjected to electrostatic discharge testing in accordance with JESD22-A114-A to check for susceptibility to damage during handling or system level assembly. Module pins were stressed at +/-2000 volt discharges using a Keytek Zapmaster automated ESD tester. Each pin was subjected to the following sequence of stress conditions:

Step	Pin Under Test	Vss Pins	Vdd Pins	Other Pins
1	3 Zaps @ + Vstress	Grounded	Floating	Floating
2	3 Zaps @ - Vstress	Grounded	Floating	Floating
3	3 Zaps @ + Vstress	Floating	Grounded	Floating
4	3 Zaps @ - Vstress	Floating	Grounded	Floating
5	3 Zaps @ + Vstress	Floating	Floating	Grounded
6	3 Zaps @ - Vstress	Floating	Floating	Grounded.

Table 8. Pins Electrostatic Discharge (ESD) Test Results

Lot Number	V-Stress	Results Fail/Tested
1	+/- 2000 V	0/5
2	+/- 2000 V	0/5
TOTAL		0/10

Latch-up Immunity

Latch-up (LU) Immunity Testing is performed to characterize the susceptibility of the device to go into a high current condition due to conduction of parasitic input devices. Latch-up testing is performed at room temperature only according to two conditions:

1. Power Supply Over Voltage - simulates a user-induced situation where a transient over-voltage is applied on the power supply.

Conditions: $> 1.5 \times V_{ddmax}$ or $I_{dd} > 120 \text{ mA}$ without Latch-up.

2. Current Injection Latch-up Test - simulates an application induced situation where the applied voltage to a pin is greater than the maximum rated conditions, such as a severe overshoot above V_{dd} or undershoot below ground on an input due to ringing. The minimum criteria for each of these conditions for a qualification are:

- a. Positive Injection: $V_{trig} > V_{dd} + 2 \times (V_{IHmax} - V_{dd})$, or $I_{trig} > 120 \text{ Ma}$
- b. Negative Injection: $V_{trig} > V_{ss} - 2 \times (V_{ss} - V_{ILmin})$, or $I_{trig} > 120 \text{ mA}$

Table 9. Latch-up Immunity Test Results

Lot Number	Overvoltage 8.25V	Current Inj. +/- 120 mA
1	0/5	0/5
2	0/5	0/5
TOTAL	0/10	0/10

Mechanical Shock & Vibration Test

This stress sequence is intended to determine the suitability of the devices for use which may be subjected to shock as a result of suddenly applied forces or abrupt changes in motion produced by rough handling, transportation or field operation. Samples are oriented in X, Y; Z planes and subjected to 1500G force for 0.5ms. The samples are then mounted on a vibration table and stress at 20G, while the frequency is swept from 20 to 2000 Hz.

Table 10. Mechanical Shock & Vibration Test Results

Lot Number	Mechanical Shock	Var. Freq. Vibration
1	0/3	0/3
2	0/3	0/3
3	0/3	0/3
TOTAL	0/9	0/9

Chemical Resistance

Samples were exposed to 12 different materials in order to verify that the coating can withstand exposure to common contaminants without adverse effects. The chemicals were applied to the surface by misting and left to dry for a 24-hour period. After drying, the sensor was cleaned with water and isopropyl alcohol and inspected for corrosion or residues. The sensors were then retested to check for deterioration in image quality. No image degradation was found. The chemicals applied in this test included:

- Tap water
- Glass cleaner (Windex®)
- Household cleaner (Formula 409®)
- Cola (Coke®)
- Coffee
- Hand crème (Oil of Olay®)
- Soap solution (5% vol. In DI water)
- Alcohol
- Gasoline (unleaded)
- Ammonia (10%)
- Hydrochloric acid (10%)
- Nitric acid (10%)
- Phosphoric acid (10%)
- Acetic acid (10%)

Mechanical Robustness Characterization

Below is a brief description for each test. Detailed results for these tests are summarized a separate document.

Pen Scratch Test:

A ballpoint pen scratch test was performed to compare the scratch resistance of coated and uncoated sensors. A BIC® fine ballpoint pen was mounted in a fixture such that the normal force exerted on the DUT could be monitored and controlled while the sensor was moved back and forth to make a scratch. The electrical image from the sensor was monitored during the scratch to detect induced damage. The coated sensors were able to withstand approximately 2x increased scratch force as compared to the uncoated controls.

Micro Scratch Test (MST) Characterization:

A Micro-Scratch Tester was also used to compare the scratch resistance of coated and uncoated sensors. This tester provided precise control with realtime closed loop feedback of the applied force and displacement speed. Characterization testing was performed with steel and diamond tips of different diameters, with progressively increasing force. The coated sensor show improve scratch resistance as compared to the uncoated sensor.

Impact Resistance Characterization:

The mechanical robustness of the sensor to impact forces was measured by dropping stainless steel balls of different diameters and mass from a controlled height. Ten (10) devices were tested for each set of test conditions, and the ball was dropped 50 times on each sample from the specified height while continuously scanning the sensor to detect induced damage. The results show that the coated sensor gives much better impact resistance as compared to the uncoated sensor.

Abrasion Resistance Characterization:

The abrasion resistance of the sensor was measured by repeatedly contacting the sensor's surface with a small piece (2 mm X 2 mm) of 120 grit sandpaper attached to a rubber eraser. An Instron Model 1123 / 5500R was programmed to perform repeated touchdowns while controlling the applied force. Fifty (50) touchdown cycles were performed at each condition, progressively increasing the contact force until failure. The results show that the coated sensor gives significantly better abrasion resistance as compared to the uncoated sensor.

Simulated Finger Touch Test

One coated sensor was subjected to over a million simulated finger touches in order to check the durability of the coating. An Instron model 1123 / 5500R was programmed to apply 2 lbs. of vertical contact force for each sensor contact. An elastomeric material was used as a simulated finger, approximating the malleable properties of the finger. The contact area of the simulated finger on the sensor surface was slightly over 95 square mm.